CMOSTEK AN147

CMT2300AW Features Usage Guideline

Summary

This document introduces some features of CMT2300AW to help users design and apply it more conveniently. The following are the RFPDK configuration interfaces and the corresponding registers associated with these features. The details of the register are introduced in the sub sections below.

The part numbers covered by this document are as shown below.

Table1. Part Numbers Covered by This Document

Part No.	Frequency	Modem	Function	Configuration	Package
CMT2300AW	127 - 1020MHz	(G)FSK/OOK	Transceiver	Register	QFN16

Before reading this document, it is recommended to read ***AN142-CMT2300AW Quick Start Guideline*** to learn the basic usage of CMT2300AW.

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1. CMT2300AW Features

The corresponding RFPDK interface and parameters are as below:

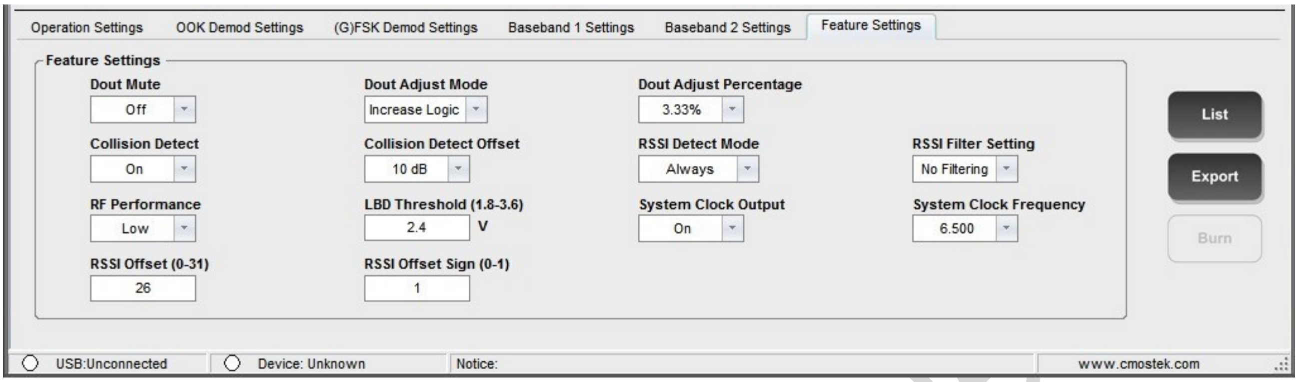

Figure1. Features RFPDK Interface

Table2. Relevant Parameters of Features

Register Bit RFPDK Parameter	Register Bit
Dout Mute	DOUT_MUTE
Dout Adjust Mode	DOUT_ADJUST_EN
Dout Adjust Mode	DOUT_ADJUST_MODE
Dout Adjust Percentage	DOUT_ADJUST_SEL<2:0>
Collision Detect	COL_DET_EN
Collision Detect Offset	COL_OFS_SEL
RF Performance	LMT_VTR<1:0> MIXER_BIAS<1:0> LNA_MODE<1:0> LNA_BIAS<1:0>
LBD Threshold	LBD_TH<7:0>

1.1 FSK Demodulation and Mute Output

Mute function is that the demodulation output has been 0 when the chip enters the RX state without signal, and the 0/1 does not flip with the noise of the bottom noise. Output as usual when there is a signal. The advantage of the mute is that if the MCU uses the demodulated output as its own wake-up input, the MCU will not be awakened without signal.

Therefore, the mute function only works in the Direct mode, that is, the client will directly configure the demodulated data to the GPIO, and uses the MCU to collect and decode the data.

In the FSK mode, the muting function is achieved by the phase hopping detection (PJD) mechanism previously introduced in the chapter of channel sensing. The user needs to configure a register to turn on the FSK mute function.

Table3. FSK Demodulation and Mute Output

Register Name	Bits	R/W	Bit Name	Function Description
CUS_SYS10 (0x15)	4	RW	DOUT_MUTE	It is valid in the FSK mode. Turn on and turn off the mute function. 0：Turn off the mute. 1：Turn on the mute.

The task of the PJD itself is to identify the useful signal and noise, and give the instruction when the useful signal is present. This instruction itself can be used as the mute enable.

1.2 Demodulation Output Duty Cycle Adjustment

The demodulation output can adjust the duty cycle of 1 and 0 by configuring the following registers. OOK and FSK share them.

Table4. Demodulation Output Duty Cycle Adjustment

Register Name	Bits	R/W	Bit Name	Function Description
CUS_CDR2 (0x2C)	4:2	RW	DOUT_ADJUST_SEL<2:0>	Percentage of duty cycle adjustment: 0：3.33% 1：6.66% 2：9.99% 3：13.32% 4：16.65% 5：19.98% 6：23.21% 7：26.64%
	1	RW	DOUT_ADJUST_MODE	Direction of duty cycle adjustment: 0：Increase the duty cycle of 1 1：Reduce the duty cycle of 1
	0	RW	DOUT_ADJUST_EN	Adjust the duty cycle of the demodulated output: 0：Disable 1：Enable

The duty cycle adjustment is centered on data 1. We can imagine the received data is the preamble, which is 10101010. Assume that the original duty cycle is 50-50. If we increase the duty cycle of 1 by 3.33%, that is, the duty cycle of all 1 in this range is changed to 53.33, and then the duty cycle of all 0 is changed to 46.67. When the data is not preamble, the length of 1 and 0 is variable, the duty cycle adjustment principle is invariant, that is, the length of the data 1 increase by 3.33% symbol, and then the length of the data 0 immediately following reduce by 3.33% symbol. No matter how many symbol the length of data 1 and 0 are, they are adjusted equally.

1.3 Fast Manual Frequency Hopping

Manual frequency hopping means that on the base frequency points obtained by the RRPDK configuration, such as 433.92MHz, it can quickly switch to another frequency point by simply setting 1 or 2 registers through the MCU in the application. Here is the associated configuration register.

Table5. Fast Manual Frequency Hopping

Register Name	Bits	R/W	Bit Name	Function Description
CUS_FREQ_CHNL (0x63)	7:0	RW	FH_CHANNEL<7:0>	Set the number of channels for fast manual frequency hopping, a total of 255 channels.
CUS_FREQ_OFS (0x64)	7:0	RW	FH_OFFSET<7:0>	Set the channel width for fast manual frequency hopping. Each bit increases by about 2.5kHz, and the maximum channel width is 2.5x255 = 637.5 kHz.

CMT2300AW effective operating frequency range is:

760– 1020 MHz
380– 510 MHz
190 – 340 MHz
127 – 170 MHz

The formula of the target frequency point is:

FREQ = Base frequency point + 2.5 kHz x FH_OFFSET<7:0> x FH_CHANNEL<7:0>

Although the basic frequency points of RX and TX are independent, the frequency hopping mechanism is only one set. The chip will switch automatically, that is, when entering the TX, the frequency hopping mechanism carries out at the basic frequency point of the TX, and when entering the RX, it carries out at the basic frequency point of the RX.

In general, the user can first configure the FH_OFFSET<7:0> at the initial stage of power-up, and then switch the channel by constantly changing the FH_CHANNEL<7:0> in the application. The user must switch the channel according to the following process:

1. Send go_stby to get the chip back to the STBY state
2. Set FH_CHANNEL<7:0>, and if the user needs to reset the FH_OFFSET<7:0>, do so in this step
3. Divide the PLL operating frequency band by reference to FREQ_DIVX_CODE<2:0> definition. If the channel is set across the frequency band, the value of the FREQ_DIVX_CODE<2:0> is reset.
4. Send go_tx into TX for transmitting, or send go_rx into RX for receiving.

The contents of these two registers are freely configured by the MCU. The chip itself does not limit whether the calculated frequency point has exceeded the frequency range that the chip can now cover. For example, the current chip is operating at 600MHz below, if the register is improperly configured, the calculation result can be more than 600MHz. Therefore, users should use their own calculation, so as not to make mistakes.

The advantage of manual FM is that users can change the frequency by setting only 1 or 2 registers. Without this mechanism, it would be necessary to write the content into the frequency bank to change the frequency. The register content to be written will increase greatly, and the time will also grow longer, which may not meet the application requirement.

1.4 Signal Collision Detection

In the environment where the interference is large and frequent, Signal Collision Detection can help the MCU identify the error in advance, allowing the MCU to save time and work on correcting error data. The following is the register for conflict detection:

Table6. Signal Collision Detection

Register Name	Bits	R/W	Bit Name	Function Description
CUS_SYS10 (0x15)	7	RW	COL_DET_EN	Signal collision detection enable 0：Disable 1：Enable
	6	RW	COL_OFS_SEL	Judgment threshold of signal conflict detection 0：10 dB 1：16 dB

The principle of channel conflict detection supported by CMT2300AW is very simple. Suppose the receiver was receiving a packet, detected a Preamble, and then successfully detected a Sync Word, and then began to receive the data behind. However, if the chip suddenly detected a suspicious Preamble at this time, it would have to process, because the Preamble should not appear again in the data behind Sync Word under normal conditions. As a result, the chip will detect the suspicious Preamble's RSSI and compare it with the previously received legal Preamble’s RSSI. If the suspicious RSSI is 10 dB or 16 dB larger than the legal RSSI (chosen by COL_OFS_SEL), confirm that this is the interference in the band. And because it is much larger than the legal data packet being received, it must have interfered the data that is being received. It immediately outputs COL_ERR interrupt to the MCU and lets the MCU handle them.

If the difference between the previous two Preamble’s RSSI is less than the threshold, it means that this might be the suspicious Preamble received currently. It's the part of the legal data package in actually. Some of the data are just like Preamble's. Because of some cases, for example, the distance between transmitter and receiver has been changed; it leads to a sudden change in RSSI. Another example, this is a real interference, but if its RSSI is less than a legal packet, 3 dB or more, it will not affect the receipt of the legal packet, so you can ignore it too.

As described earlier in the chapters on GPIO and interruption, after the COL_ERR interrupt carry out logic OR with PKT_ERR and PKT_OK, it will generate the PKT_DONE interrupt and output it to the MCU. When the MCU receives this interrupt, the first thing is to query the flag bit to determine which interrupt source is triggered, If the COL_ERR is triggered, the FIFO data being read can be discarded, The data must have been wrong because it was aware of the interference, and then exit RX and re-enter RX to receive. The advantage is that the MCU does not have to wait until all data packets are received before it knows the data is wrong. Early processing can save electricity and time.

1.5 Receiver RF Current Regulation

The CMT2300AW provides a set of registers for the user to reduce the RF current of the receiver, but the performance will also decrease accordingly. Here are the associated registers:

Table7. Receiver RF Current Regulation

Register Name	Bits	R/W	Bit Name	Function Description
CUS_SYS1 (0x0C)	7:6	RW	LMT_VTR<1:0>	LMT VTR current level
	5:4	RW	MIXER_BIAS<1:0>	Mixer current level
	3:2	RW	LNA_MODE<1:0>	LNA current level 1
	1:0	RW	LNA_BIAS<1:0>	LNA current level 2

The cost of reducing current is that the RF performance decreases accordingly. The following is the configuration method for the 4 registers:

Table8. Configuration Method of Current Register

Current level	RF performance level	LMT_VTR<1:0>	MIXER_BIAS<1:0>	LNA_MODE<1:0>	LNA_BIAS<1:0>
Low	Low	2	2	1	1
Middle	Middle	2	2	1	2
High	High	1	2	3	2

1.6 Low Battery Detection（LBD）

CMT2300AW provides the LBD function. Here are the associated registers:

Table9. Low Battery Detection- Register Located in the Configuration Bank

Register Name	Bits	R/W	Bit Name	Function Description
CUS_LBD (0x5F)	7	RW	LBD_TH<7:0>	LBD contrast threshold

Table10. Low Battery Detection- Register Located in the Control Bank2

Register Name	Bits	R/W	Bit Name	Function Description
CUS_LBD_RESULT (0x71)	7	RW	LBD_RESULT<7:0>	LBD test result

LBD operation principle is that the LBD_TH set by the user represents the threshold of LBD. The formula is as follows:

$$VTH = LBD\_TH / 255 \times 4.8\ V$$

In dealing with LBD, the chip first measures the voltage of the VDD and converts it to LBD_RESULT in accordance with the same formula:

$$VDD = LBD\_RESULT / 255 \times 4.8\ V$$

As the chip gets the measurement result, it will compare the LBD_RESULT with the LBD_TH. If LBD_RESULT is found to be smaller than LBD_TH, then a low voltage has occurred, and a valid interrupt of LBD will be output to notify the outside MCU. It is recommended that MCU clear this interrupt immediately and proceed further. On the other hand, CMT2300AW's LBD is not real-time, and there is no specific command to execute LBD. It will be checked while the PLL is correcting the frequency point. PLL frequency point correction will occur when the following 2 states are switched:

1. SLEEP/STBY switch to RFS/RX
2. SLEEP/STBY switch to TFS/TX

1.7 Chip Error State Processing

Table11. ERROR State Processing Register

Register Name	Bits	R/W	Bit Name	Function Description
CUS_EN_CTL (0x62)	5	RW	ERROR_STOP_EN	Some internal errors occur when the chip encounters an unexpected strong interference. At this point, the user can choose to make the chip unable to access TX or RX, and stay in the state 1000, and wait for the MCU to switch the chip back to the STBY state. This bit is the enable bit of this function. 0：Disable，switch the state as usual 1：Enable

In general, if the chip is in a state of error and continues into the TX state, it will cause the spectrum confusion and interfere with the surrounding wireless devices. At the same time, this will also benefit the product through the ETSI standard. Therefore, it is strongly recommended that users open this feature so that the MCU can handle the chip in an error state. For more information, please refer to the description and the Demo program given in the《AN142-CMT2300AW quick start guideline》.

2. Document Modification Record

Table10. Document Modification Record Sheet

Version	Chapter	Modification descriptions	Date
0.8	All	Initial release version	2017-03-24
0.9	Summary	Add the advice to read AN142	2017-07-12
	The first chapter	Remove the LBD_STOP_EN correlation description because this function is useless. Rename the PLL lock processing to chip error state processing. Rename UNLOCK_STOP_EN to ERROR_STOP_EN and update the relevant description.	
	All	Revise individual typos	

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